International Journal of
Science and Engineering Investigations vol. 11, issue 122, March 2022
Received on March 9, 2022 ISSN: 2251-8843

An Improved ESOP-Based Method for Synthesizing the Reversible Circuit Using Mixed-Polarity Toffoli Gate

Hieu Nguyen[1], Hiep Luu[2], Linh Tran[3]
[1,2,3]Department of Electronics, Ho Chi Minh City University of Technology (HCMUT), Ho Chi Minh City, Vietnam
[1,2,3]Department of Electronics, Vietnam National University Ho Chi Minh City (VNU-HCM), Ho Chi Minh City, Vietnam
([1]hieunt@hcmut.edu.vn, [2]1751031@hcmut.edu.vn, [3]linhtran@hcmut.edu.vn)

Abstract- This study introduced an improved ESOP-based algorithm for synthesizing the reversible circuit. The ESOP-based algorithms require fewer ancilla lines but more quantum costs and gate costs differentiating from other methods used for synthesis. We proposed a new version of the EPOEM-1 algorithm (an ESOP-based algorithm) called EPOEM-1* by combining it with the Mixed-polarity Toffoli gates. The new algorithm inherits the pros of the ESOP-based methods and reduces the cost by the properties of the gates. The experimental results show that the improved method brings better costs in most cases.

Keywords- *ESOP-Based, EPOEM, Mixed-Polarity Tofolli Gate, Reversible Circuit, Synthesis*

I. INTRODUCTION

Over the last two decades, many studies proved the critical role of this type of circuit in many fields such as quantum computing [1]–[3], DNA computing [1], optical computing [4], and in nanotechnology [5]. Because of its future necessity and importance, synthesis of reversible logic circuits has become a trending topic. Compared with the irreversible traditional circuit which processes the bits (0,1), the qubits are the processed objects of the reversible circuit [1], [6]. It leads to the reversible logic gates which are the main structures of this circuit. Besides, the reversible circuit synthesis faces two main problems: fanout and feedback. Only cascade structures can handle both issues. For the above reasons, many techniques for synthesis reversible circuit has been researched and developed, for instance, transformation-based, search-based, cycle-based, BDD-based and ESOP-based methods.

In [7], [8], Maslov et. al proposed the transformation-based method. This method chooses a reversible gate (Toffoli, Fredkin, …) and relies on the properties of this gate to transform the truth table sequentially to synthesize the circuit. The following method is the search-based method (or also called the heuristic method) [9]–[11]. This method has two phases: first, it finds the possible path selection iteratively using Hamming distance [12]. Second, it selects the possible reversible gates based on the first phase's results. Both methods relying on the size of the truth table leads to increasing processing time when the numbers of inputs are increased. In [13], [14], Saeedi et al. introduced cycle-based method. This method's main idea is decomposing the Boolean functions into smaller cycles and synthesizing them into a circuit. Its results depend on the decomposition process (the chosen gates, the number of cycles,…). Unlike these techniques which are not scalable for very large input benchmark circuits, the BDD and ESOP-based methods are proven very efficient for larger circuits. Wille et. al. first introduced the BDD-based method in [15]. The first step of this method is building a BDD (Binary Decision Diagram) [16] from the Boolean functions. Then, traveling all nodes of the BDD and matching each node to a cascade of reversible gates. This method can apply to the large function with up to huge variables input in a short time [15], which is the weakness of previous methods. On the other hand, the results of this method have many garbage lines compared with the other method. Because of the shared node's properties of BDD, adding new templates to the resulting circuit leads to increasing more lines of the circuit.

Our study starts from the ESOP-based method. Many studies have proposed it [17]–[27] as a highly scalable synthesis. There are many ESOP-based algorithms introduced, for instance: ESOP-based Toffoli network [21], ESOP cubes [23], [24], EXOR-sum of Products-of-EXOR-sums (EPOE) method [25]–[27], …The most impressive method is EPOE because of the minimum cost metric compared with the others. There are two variants called EPOEM-1 and EPOEM-2, respectively. The EPOEM-1 has two phases: building EPOE gate structures (templates) from Boolean input specifications and choosing the suitable EPOE structures to synthesize. The EPOEM-2 needs to create the library of templates in advance. Comparing two variants, the EPOEM-1 takes the best cost. Our motivation is to combine the EPOEM-1 with the Mixed-polarity Toffoi gates to create a new structure to decrease the quantum cost. These gates comprise the Toffoli gate, Semi-controlled Toffoli gate and Negative-controlled Toffoli gate, which were studied in [14], [28], [29] and used with search-based, cycle-based and BDD-based methods. The usage of the Mixed-polarity Toffoi gates was proven to reduce the cost of the circuit.

The rest of this paper is summarized into three main parts: first, we propose the basic definition of reversible function and circuit, the theory of ESOP-based synthesis and our approach using the Mixed-polarity Toffoli gate. Next, we proposed an improved algorithm called EPOEM-1*, which combines the classical EPOEM-1 algorithm and the properties of the Mixed-polarity Toffoli gate. Finally, we show the experimental results and discussion about our technique.

II. PRELIMINARIES

A. *Reversible function*

A mapping $f : B^n \rightarrow B^m$ is a multiple-output reversible function if satisfying two conditions: the number of input equals the number of output (n = m) and any input only maps to a unique output. Based on this definition, any irreversible function with n input and m < n output becomes reversible when adding (n-m) value to output called ancilla line.

B. *Reversible circuit and reversible gate*

A reversible circuit realizes a reversible function which means all the inputs and outputs of the circuits have to satisfy the conditions of a reversible function. This circuit is constructed by connecting a set of elements called reversible gates. Reversible gates also have the number of inputs equal to the number of outputs, one of two main constraints of reversible function.

In general, a reversible gate expresses a multiple-output function $g:B^a \rightarrow B^a$. Let denote $C = \{c_1, c_2, ..., c_a\} \subset X$ and $D = \{d_1, d_2, ..., d_b\} \subset X$ with $C \cap D = \varnothing$, in which C is called the set of control lines and D is called the set of target lines. This research focuses on the Toffoli gate and the Mixed-polarity Toffoli gate. Using the mapping definition, the Toffoli gate has the function g map:

$\{x_1, x_2, ..., x_{n-1}, x_n\}$ to $\{x_1, x_2, ..., x_{n-1}, x_n \oplus x_1 x_2 ... x_{n-1}\}$

The definition of the Mixed-polarity Toffoli is similar, with NOT operating at the target line. Some examples of two types of gates with 3-bit are shown in Fig. 1.

- 3-bit Toffoli gate (Figure 1a): expresses the function map $\{x_1, x_2, x_3\}$ to $\{x_1, x_2, x_3 \oplus x_1 x_2\}$

- Semi-negative 3-bit Toffoli gate (Figure 1b): the function map $\{x_1, x_2, x_3\}$ to $\{x_1, x_2, x_3 \oplus \overline{x_1} x_2\}$

- Negative 3-bit Toffoli gate (Figure 1c): the function map $\{x_1, x_2, x_3\}$ to $\{x_1, x_2, x_3 \oplus \overline{x_1 x_2}\}$

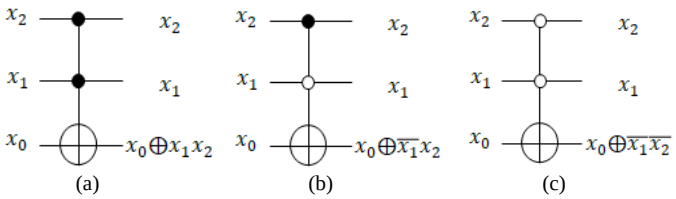


Figure 1. The Toffoli gate and mixed-polarity Toffoli gate.

C. *Evaluating synthesis circuits*

There are many ways to realize a reversible function in the circuit. Three common parameters used to evaluate the resulting circuit and the synthesis algorithm are gate count (GC), quantum cost (QC) and the ancilla lines (L.). Gate count is the number of gates in a circuit. The quantum cost is defined as the number of basic quantum operations needed to realize the gate [12]. The quantum cost of the 3-bit gate in Fig. 1 is 5, 5, and 7, respectively. In general, the quantum cost increases when the number of control bits increases. In general, the quantum cost of some Toffoli gates is shown in Table I. [30]

TABLE I. THE QUANTUM COST OF TOFFOLI GATE AND MIXED-POLARITY TOFFOLI GATE.

Gate	QC
CNOT (2-bit Toffoli gate)	1
Negative CNOT	3
3-bit Toffoli gate	5
Semi-negative 3-bit Toffoli gate	5
Negative 3-bit Toffoli gate	7
n-bit Toffoli gate	2^n-3
Semi-negative n-bit Toffoli gate	2^n-3
Negative n-bit Toffoli gate	2^n-1

D. *Using mirror circuit to eliminate the garbage output*

Based on the algorithm used to synthesize the reversible function, some results need to add more ancilla lines when the others do not. Fig. 2 shows two resulting circuits of function. A circuit with three ancilla lines is shown in Fig. 2a. One of them is set to function *f* at the output when the others are not – called garbage line. Moreover, lines a and c_1 also do not hold the same value at the output, which leads the circuit to become unreversible. In Fig. 2b, a circuit with no garbage lines is shown. This circuit has mirror circuits to restore the values of input lines. It is achieved by taking the outputs of the reversible circuit and producing them inversely.

Calculating the mirror circuit of the function *f* is essentially the same operation as propagating this pattern backward through the circuit. Hence, if the cascade of *n* reversible gates $G = g_0 g_1 ... g_{n-1}$ realizes a reversible function *f*, the reverse cascade $G = g_{n-1} g_{n-2} ... g_0$ realizes the mirror circuit of function *f*.

Using mirror circuits reduces the usage of the ancilla line and increases the quantum cost [31].

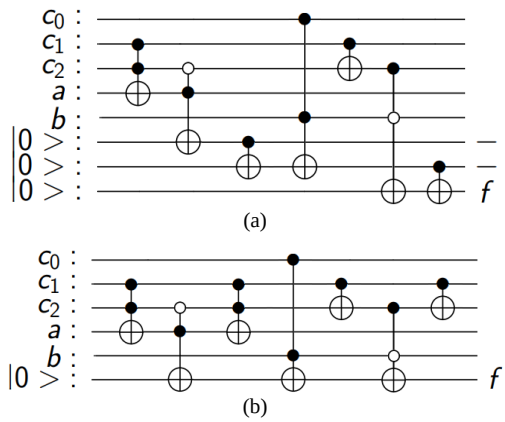


Figure 2. Two realization circuits for function *f*.

E. Theory of ESOP-based synthesis

An exclusive-or-sum-of-product (ESOP) which uses the exclusive-or-sum ($\oplus$) operator is a variation of the sum of products (SOP) in boolean function representation. In [32], any boolean function can be converted into an equivalent ESOP form:

$$f(x_1, x_2, ..., x_n) = c_0 \oplus c_1 x_1 \oplus ... \oplus c_n x_n \oplus c_{12} x_{12} \oplus ... \oplus c_{n-1,n} x_{n-1} x_n \oplus ... \oplus c_{1,2,...,n-1,n} x_1 ... x_{n-1} x_n \quad (1)$$

This expression is also called PPRM (Positive Polarity Reed-Muller) expression. In [27], the author introduces an algorithm called EPOEM-1 to synthesize the reversible circuit. This algorithm has two phases:

- Phase 1, creating product-of-exclusive-sum (POE) templates. These templates are divided into many *N* levels $0, 1, 2, ..., N-1$. The templates at each level cover $2^{N-level}$ minterms and are expressed into POE form.
- Phase 2, at each level, choose a suitable template that covers $2/3$ the minterms of the function. Exor all the chosen ones to get the result.

In PPRM form, $x \oplus 1$ is used instead of $\bar{x}$. It leads to using a NOT gate when synthesizing the circuit. By using another form called MPRM (Mixed Polarity Reed-Muller) expression [33], the usage of NOT gate can reduce. This expression is similar to (1), except $x_1, x_2, ..., x_n$ can have NOT operator or no operator.

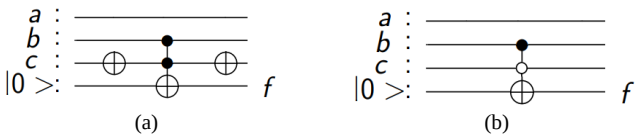


Figure 3. Two realization circuits for function f using PPRM and MPRM expressions.

Fig. 3 shows the circuits that are realized for the PPRM expression (a) and MPRM expression (b). The circuit in Fig. 3a has a GC and a QC of 3 and 5, respectively. On the other hand, by using the mixed-Toffoli gate, the GC and QC reduce to 1 and 5 in Fig. 3b.

III. ALGORITHM

In this study, combining the EPOEM-1 algorithm with the realization using the Toffoli and the mixed-Toffoli gates, we develop a new version of this algorithm called EPOEM-1*. Because the new version uses another type of gate, the cost used for choosing templates is re-calculated.

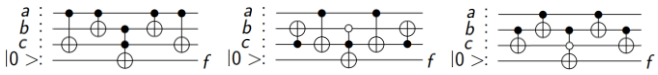
A. The QC of POE templates using the Toffoli and the Mixed-polarity Toffoli gate

The EPOEM-1 algorithm uses two types of template libraries called the single expression library and the full expression library. Both libraries share all the templates at levels 0 and 1 but differ in their levels 2 and higher. The single template is chosen by calculating and finding the minimum quantum cost of all templates in the full template. An example of the POE templates of three variables is shown in Table II.

TABLE II. EXAMPLES OF POE TEMPLATE EXPRESSIONS FOR FUNCTIONS OF THREE VARIABLES.

Level	Template	POE Template expressions	
		Single expression template library	Full expressions template library
0	{000,001,010,011, 100,101,110,111}	1	1
1	{100,101,110,111}	a	a
1	{010,011,100,101}	$a \oplus b$	$a \oplus b$
1	{001,010,100,111}	$a \oplus b \oplus c$	$a \oplus b \oplus c$
2	{100,101}	$a(a \oplus b)$	$a(a \oplus b)$;$a(b \oplus 1)$; $(a \oplus b)(b \oplus 1)$
2	{100,011}	$(a \oplus c)(a \oplus b)$	$(a \oplus c)(a \oplus b)$; $(a \oplus c)(b \oplus c \oplus 1)$; $(a \oplus b)(b \oplus c \oplus 1)$

With the synthesis method using the Mixed-polarity Toffoli gate, the single template changes and can be unnecessary to calculate. Fig. 4 shows three realization circuits of template {100,011}. All circuits have the QC of 9.



(a) (b) (c)

Figure 4. The realization circuits for template {100,011}.

We calculate the cost for each template in the full template library to find the minimum cost template. In general, let N is the number of variables of the function. Assume that level i is considered ($i = 2,..., N-1$).

- The level i has the product of i exclusive-or elements. It leads to using $(i+1)$ bit Toffoli gates or $(i+1)$ bit Mixed-polarity Toffoli gates. The QC for this gate at level i is $2^{i+1}-1$ (if the negative gate is used) or $2^{i+1}-3$ (if the others are used).
- Each exclusive-or element can be a variable or an exclusive-or of variables. If it is only a variable, no more gate is used. In case there are n variables $(1 < n \le N)$, $n-1$ CNOT gate is used. We need the mirror circuit to construct the reversible circuit, the QC is $2(n-1)$.

The total quantum cost for each template in the full template library is the sum of the two results above.

*B. Algorithm EPOEM-1**

Denote *ON_set* is the set of all minterms of the input function, *Results_set* is the set of all chosen POE from the full template library.

The pseudocode for our algorithm is described.

More details about the algorithm are shown in the example.

Example: Using the proposed algorithm to synthesize the function: $f(a,b,c,d) = \{5,6,7,8,9,10,11,12,13,14,15\}$

- Initial ON_set={5,6,7,8,9,10,11,12,13,14,15}
- Initial $N = 4$
- Initial Results_set := $\varnothing$
- Because length(*ON_set*)=11 $> \frac{2}{3}2^4$ then

  Results_set has first NOT_gate,

  ON_set=set_1 sub ON_set = {0,1,2,3,4}

Algorithm EPOEM-1*

1: Initial *ON_set* from the function

2: Initial N := numbers of variables

3: Initial *Results_set* := $\varnothing$

4: Initial *Level* := 1 *//Level in the template library*

4: If length(*ON_set*) $> \frac{2}{3}2^N$ then

5: *Results_set.append(NOT_gate)*

6: *ON_set := set_1 sub ON_set*

7: For *Level* := 1 to $N-1$:

8: *temp_set* := $\varnothing$ *//Temporarity set*

9: For *each_template* in *the_full_template_library*:

10: If length(intersection(*ON_set*,*each_template*)) $\ge \frac{2}{3}2^{N-level}$:

11: temp_set.append(*each_template)*

12: While (condition == run):

13: For *each_template* in *temp_set*:

13: Find all the template which have the largest intersection with *ON_set*

14: Choose the template with the best quantum cost *//calculate using 3.1*

15*:* *Results_set.append(chosen_template))*

16: *temp_set*.remove(*chosen_template*)

17: If length(*temp_set) == 0:*

18: condition:=stop

- At *level 1:* there are no templates covering $\frac{2}{3}$ the *ON_set*. Move to step *level 2*

- At *level 2:* there are 3 templates covering $\frac{2}{3}$ the *ON_set.* They are $\bar{a}\bar{b}$, $\bar{a}\left(\overline{a \oplus b}\right)$ and $\bar{b}\left(\overline{a \oplus b}\right)$. The length of intersection set between each of them and *ON_set* is 3. Calculate the QC of each template. The first template $\bar{a}\bar{b}$ has the QC of 7. Two others have the QC of 9. The template has the minimum QC is $\bar{a}\bar{b}$.

  Results_set has template $\bar{a}b$

  ON_set = {4}

- At *level 3*: only 1 template satisfies the condition. It is $\bar{a}bc\bar{d}$

  The resulting circuit is: $f = \overline{\bar{a}\bar{b} \oplus \bar{a}bc\bar{d}}$

The realization circuit is shown in Fig. 5. The total quantum cost of this circuit is 37.

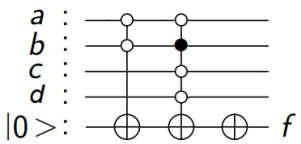


Figure 5. The realization circuit of example

The main difference between the EPOEM-1 and the EPOEM-1* algorithm is the step calculation of the quantum cost of each template in the full template library. This step uses the Mixed-polarity Toffoli gates for the synthesis process, which reduces the quantum cost of the circuit. In the algorithm, the Fractional Covering Criterion $\frac{2}{3}$ is used. It is proven in [27].

C. Bounding value of the algorithm

From section 3.1, the QC for each template at level i is $2^{i+1}-1+2(n-1)$ (if the negative gate is used) or $2^{i+1}-3+2(n-1)$ (if the others are used). $(1<n\le N)$, N: numbers of variables.

The worst QC for each template at level i is:

$$2^{i+1}-1+2(N-1)=2^{i+1}+2N-3.$$

The algorithm fetches from level 1 to level $N-1$. The worst case is that all minterms are chosen at the level $N-1$. Denote a is the number of minterms of the input function. The worst QC of our algorithm is:

$$a\left(2^{N-1+1}+2N-3\right)=a\left(2^{N}+2N-3\right).$$

Similarity, the GC for each template at level i is $1+2(n-1)$. The worst GC of our algorithm is:

$$a(1+2(N-1))=a(2N-3).$$

The ancilla line used in our algorithm is 1 in case 1-variable functions and none in case multiple-variable functions.

IV. RESULTS AND DISCUSSION

This section shows our evaluation of the experimental results of our algorithm. Our proposed algorithm is implemented by using Python. Our benchmarks functions are provided by RevLib [34]. The parameters for these tests are quantum cost (QC). All experiments have been carried out on a personal laptop with an Intel Core i7 processor, 1.8GHz, and 8GB RAM. The result is shown in Table III.

The full template library used to evaluate our algorithm is proposed in [27]. In this test, we also show the results of functions which is used in the previous study [27], [17], [18], and [35].

TABLE III. TABLE OF RESULTS.

Function	EPOEM-1*	EPOEM-1 [27]	[17]	[35]	[18]
4gt4_20	**37**	45	45	45	45
4gt5_21	**14**	16	16	16	16
4gt10_22	**34**	36	36	41	36
4gt11_23	5	5	5	5	5
4gt12_24	**34**	38	44	38	38
4gt13_25	13	13	13	13	13
4mod5_8	**11**	13	28	28	13
4sf_232	**27**	31	38	40	27
sym6	**120**	136	857	-	-
8newill	**675**	684	1239	-	-
8newtag	**480**	483	683	-	-
8rd84f1	60	60	277	-	-
8rd84f2	8	8	24	-	-
8rd84f3	**497**	509	509	-	-
8rd84f4	**330**	333	4824	-	-
5alu_9	**27**	39	52	119	-
5ex2_151	**85**	93	143	-	-
5ex3_152	**61**	69	84	84	-
5majority	**98**	112	149	149	-
5rd53f1	**67**	69	177	185	-
5rd53f2	25	25	88	-	-
5xor5	**9**	**9**	**9**	**13**	-
7con1f1	**113**	**119**	**141**	-	-
7con2f2	**50**	**60**	**68**	-	-
7rd73f1	**118**	**150**	**211**	-	-
7rd73f2	**13**	**13**	**19**	-	-
7rd73f3	**181**	**203**	**1337**	-	-

Comparing the QC of our proposed method with the others, the minimum cost is made bold. The results show that our algorithm has less cost in most cases. In the other cases, the function finds from the EPOEM-1 and the EPOEM-1* are the same, which means there are no NOT operators in the resulting function. For example, the benchmark *4gt11_23* gives the result: $f=ab$. Our algorithm cannot improve the cost because there are no usage NOT gates.

The EPOEM-1 algorithm is better than the [17], [18], and [35]. Then, our proposed method brings better results than the EPOE-1M.

V. CONCLUSION

In this paper, an improved algorithm of EPOEM-1 called EPOEM-1* is introduced. This method is a combination of the EPOEM-1 with the Mixed-polarity Toffoli gate. Our algorithm is expected to reduce all parameters: GC and QC. The experimental results in Section 4 show that our algorithm has

better results in reducing QC compared with previous algorithms. Our algorithm also has a trade-off between QC of the complexity of the algorithm.

ACKNOWLEDGEMENTS

This research is funded by Ho Chi Minh City University of Technology (HCMUT), VNU-HCM under grant number To-DDT-2020-10. We acknowledge the support of time and facilities from Ho Chi Minh City University of Technology (HCMUT), VNU-HCM for this study.

REFERENCE

[1] C. H. Bennett, "Logical Reversibility of Computation," *IBM J. Res. Dev.*, vol. 17, no. 6, pp. 525–532, Nov. 1973, doi: 10.1147/rd.176.0525.

[2] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM J. Res. Dev.*, vol. 5, no. 3, pp. 183–191, Jul. 1961, doi: 10.1147/rd.53.0183.

[3] M. Swathi and B. Rudra, "Implementation of Reversible Logic Gates with Quantum Gates," in *2021 IEEE 11th Annual Computing and Communication Workshop and Conference (CCWC)*, NV, USA, Jan. 2021, pp. 1557–1563. doi: 10.1109/CCWC51732.2021.9376060.

[4] R. Cuykendall and D. R. Andersen, "Reversible optical computing circuits," *Opt. Lett.*, vol. 12, no. 7, p. 542, Jul. 1987, doi: 10.1364/OL.12.000542.

[5] J. S. Hall, "Nanocomputers and reversible logic," *Nanotechnology*, vol. 5, no. 3, pp. 157–167, Jul. 1994, doi: 10.1088/0957-4484/5/3/002.

[6] C. Sharma, H. Pahuja, M. Dadhwal, and B. Singh, "Study of Reversible Logic Synthesis with Application in SOC: A Review," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 225, p. 012250, Aug. 2017, doi: 10.1088/1757-899X/225/1/012250.

[7] D. M. Miller, D. Maslov, and G. W. Dueck, "A transformation based algorithm for reversible logic synthesis," in *Proceedings of the 40th conference on Design automation - DAC '03*, Anaheim, CA, USA, 2003, p. 318. doi: 10.1145/775832.775915.

[8] D. Maslov, "Linear depth stabilizer and quantum Fourier transformation circuits with no auxiliary qubits in finite-neighbor quantum architectures," *Phys. Rev. A*, vol. 76, no. 5, p. 052310, Nov. 2007, doi: 10.1103/PhysRevA.76.052310.

[9] P. Gupta, A. Agrawal, and N. K. Jha, "An Algorithm for Synthesis of Reversible Logic Circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 11, pp. 2317–2330, Nov. 2006, doi: 10.1109/TCAD.2006.871622.

[10] J. Donald and N. K. Jha, "Reversible logic synthesis with Fredkin and Peres gates," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 4, no. 1, pp. 1–19, Mar. 2008, doi: 10.1145/1330521.1330523.

[11] S. C. Chua and A. K. Singh, "Search-Based Reversible Logic Synthesis Using Mixed-Polarity Gates," in *Design and Testing of Reversible Logic*, vol. 577, A. K. Singh, M. Fujita, and A. Mohan, Eds. Singapore: Springer Singapore, 2020, pp. 93–113. doi: 10.1007/978-981-13-8821-7_6.

[12] D. Maslov and G. W. Dueck, "Reversible Cascades With Minimal Garbage," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 23, no. 11, pp. 1497–1509, Nov. 2004, doi: 10.1109/TCAD.2004.836735.

[13] M. Saeedi, M. S. Zamani, M. Sedighi, and Z. Sasanian, "Reversible circuit synthesis using a cycle-based approach," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 6, no. 4, pp. 1–26, Dec. 2010, doi: 10.1145/1877745.1877747.

[14] M. Saeedi, M. Sedighi, and M. Saheb Zamani, "A library-based synthesis methodology for reversible logic," *Microelectron. J.*, vol. 41, no. 4, pp. 185–194, Apr. 2010, doi: 10.1016/j.mejo.2010.02.002.

[15] R. Wille and R. Drechsler, "BDD-based synthesis of reversible logic for large functions," in *Proceedings of the 46th Annual Design Automation Conference on ZZZ - DAC '09*, San Francisco, California, 2009, p. 270. doi: 10.1145/1629911.1629984.

[16] Bryant, "Graph-Based Algorithms for Boolean Function Manipulation," *IEEE Trans. Comput.*, vol. C–35, no. 8, pp. 677–691, Aug. 1986, doi: 10.1109/TC.1986.1676819.

[17] N Alhagi, M. Lukac, L. Tran, and M. Perkowski, "Two-stage approach to the minimization of quantum circuits based on ESOP minimization and addition of a single ancilla qubit," 2012, pp. 25–36.

[18] C. Bandyopadhyay, D. Roy, D. K. Kole, K. Datta, and H. Rahaman, "ESOP-Based Synthesis of Reversible Circuit Using Improved Cube List," in *2013 International Symposium on Electronic System Design*, Singapore, Dec. 2013, pp. 26–30. doi: 10.1109/ISED.2013.12.

[19] K. Fazel, M. A. Thornton, and J. E. Rice, "ESOP-based Toffoli Gate Cascade Generation," in *2007 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, Victoria, BC, Canada, Aug. 2007, pp. 206–209. doi: 10.1109/PACRIM.2007.4313212.

[20] Y. Sanaee and G. W. Dueck, "Generating Toffoli networks from ESOP expressions," in *2009 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, Victoria, BC, Canada, Aug. 2009, pp. 715–719. doi: 10.1109/PACRIM.2009.5291282.

[21] Y. Sanaee and G. W. Dueck, "ESOP-Based Toffoli Network Generation with Transformations," in *2010 40th IEEE International Symposium on Multiple-Valued Logic*, Barcelona, Spain, 2010, pp. 276–281. doi: 10.1109/ISMVL.2010.58.

[22] J. E. Rice and V. Suen, "Using autocorrelation coefficient-based cost functions in ESOP-based Toffoloi gate cascade generation," in *CCECE 2010*, Calgary, AB, Canada, May 2010, pp. 1–6. doi: 10.1109/CCECE.2010.5575167.

[23] J. E. Rice and N. M. Nayeem, "Ordering techniques for ESOP-based Toffoli cascade generation," in *Proceedings of 2011 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, Victoria, BC, Canada, Aug. 2011, pp. 274–279. doi: 10.1109/PACRIM.2011.6032905.

[24] N. Nayeem and J. Rice, "A shared-cube approach to ESOP-based synthesis of reversible logic," *Facta Univ. - Ser. Electron. Energ.*, vol. 24, no. 3, pp. 385–402, 2011, doi: 10.2298/FUEE1103385N.

[25] L. Tran, A. Gronquist, M. Perkowski, and J. Caughman, "An Improved Factorization Approach to Reversible Circuit Synthesis Based on EXORs of Products of EXORs," in *2016 IEEE 46th International Symposium on Multiple-Valued Logic (ISMVL)*, Sapporo, Japan, May 2016, pp. 37–43. doi: 10.1109/ISMVL.2016.56.

[26] L. Tran, B. Yen, and M. Perkowski, "Comparison of various error-detecting and error-correcting encodings of reversible automata built from irreversible state tables using EPOE circuits with EXOR lattices," in *2017 International Conference on Information and Digital Technologies (IDT)*, Zilina, Slovakia, Jul. 2017, pp. 390–399. doi: 10.1109/DT.2017.8024327.

[27] L. Tran, B. Schaeffer, A. Gronquist, M. Perkowski, and P. Kerntopf, "Synthesis of Reversible Circuits Based on EXORs of Products of EXORs," in *Transactions on Computational Science XXIV*, vol. 8911, M. L. Gavrilova, C. J. K. Tan, H. Thapliyal, and N. Ranganathan, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2014, pp. 111–128. doi: 10.1007/978-3-662-45711-5_7.

[28] C. S. Cheng, A. K. Singh, and L. Gopal, "Efficient Three Variables Reversible Logic Synthesis Using Mixed-polarity Toffoli Gate," *Procedia Comput. Sci.*, vol. 70, pp. 362–368, 2015, doi: 10.1016/j.procs.2015.10.035.

[29] H. Nguyen and L. H. Tran, "Synthesis of Reversible and Quantum Circuit Using ROCBDD and Mixed-Polarity Toffoli Gate," *IEEE Access*, vol. 9, pp. 135432–135439, 2021, doi: 10.1109/ACCESS.2021.3116756.

[30] D. Maslov, G. W. Dueck, D. M. Miller, and C. Negrevergne, "Quantum Circuit Simplification and Level Compaction," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 27, no. 3, pp. 436–444, Mar. 2008, doi: 10.1109/TCAD.2007.911334.

[31] D. M. Miller, R. Wille, and R. Drechsler, "Reducing Reversible Circuit Cost by Adding Lines," in *2010 40th IEEE International Symposium on Multiple-Valued Logic*, Barcelona, Spain, 2010, pp. 217–222. doi: 10.1109/ISMVL.2010.48.

[32] T. Sasao and D. Dednath, "An exact minimization algorithm for generalized Reed-Muller expressions," in *Proceedings of APCCAS'94 - 1994 Asia Pacific Conference on Circuits and Systems*, Taipei, Taiwan, 1994, pp. 460–465. doi: 10.1109/APCCAS.1994.514594.

[33] X. Wang et al., "Polarity Searching for MPRM Logic Circuit Based on Improved Adaptive Genetic Algorithm," in 2015 IEEE 12th Intl Conf on Ubiquitous Intelligence and Computing and 2015 IEEE 12th Intl Conf on Autonomic and Trusted Computing and 2015 IEEE 15th Intl Conf on Scalable Computing and Communications and Its Associated Workshops (UIC-ATC-ScalCom), Beijing, Aug. 2015, pp. 1354–1358. doi: 10.1109/UIC-ATC-ScalCom-CBDCom-IoP.2015.244.

[34] R. Wille, D. Gro, L. Teuber, G. W. Dueck, and R. Drechsler, "RevLib: An Online Resource for Reversible Functions and Reversible Circuits," in *38th International Symposium on Multiple Valued Logic (ismvl 2008)*, Dallas, TX, USA, May 2008, pp. 220–225. doi: 10.1109/ISMVL.2008.43.

[35] "Comparison of Maslov's Quantum Costs and LNNM Quantum Costs for Four Types of Multi-qubit Toffoli Gates," 2012, pp. 81–87.

[36] R. Wille and R. Drechsler, "Effect of BDD Optimization on Synthesis of Reversible and Quantum Logic," *Electron. Notes Theor. Comput. Sci.*, vol. 253, no. 6, pp. 57–70, Mar. 2010, doi: 10.1016/j.entcs.2010.02.006.

How to Cite this Article:

Nguyen, H., Luu, H. & Tran, L. (2022). An Improved ESOP-Based Method for Synthesizing the Reversible Circuit Using Mixed-Polarity Toffoli Gate. International Journal of Science and Engineering Investigations (IJSEI), 11(122), 14-20. http://www.ijsei.com/papers/ijsei-1112222-03.pdf