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Rail-to-Rail Op-Amp Design Incorporating Negative Miller and Miller Compensation

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Abstract-This paper considers and presents the design of a rail-to-rail input and output CMOS (complementary metal oxide semiconductor) two-stage operational amplifier (op-amp). The design uses two capacitance based compensation techniques for controlling stability and frequency response, the conventional Miller and negative Miller capacitances. The negative Miller capacitance is constructed around the first amplification stage and the conventional Miller capacitance is constructed around the second amplification stage. By setting suitable capacitance values, the conventional Miller and negative Miller capacitances allow the designer to control stability margins and frequency response. The design is based on a low-power design where the first stage consists of complementary differential input and summing circuit, and the second stage is a class-AB amplifier. The design has been created using a 0.35 µm CMOS (n-well) technology, its operation strategy simulated using the Cadence Spectre simulator and operates on a +3.3 V power supply.

Keywords-*Miller Compensation, Negative Miller, Rail-to-Rail Amplifier, Constant-g_m, Class AB Amplifier*

I. INTRODUCTION

The op-amp consists of a differential signal amplification input stage with a differential or single-ended output amplification stage and would be designed to operate on a dual- or single-rail power supply voltage. The op-amp is an important circuit in many analog and mixed-signal integrated circuits (ICs). To design for low-power and low-voltage operation requires a decrease in the op-amp power supply voltage. However, lowering the power supply voltage results in a decrease in the AC, DC and transient performance of the op-amp when compared to the operation of the circuit at higher voltage levels. It is therefore necessary to identify the performance parameters of interest and to ensure that these can be attained. In this paper, consideration is given the op-amp operation using single +3.3 V power supply and circuit operation is considered to be compatible with standard +3.3 V circuit operation. Therefore, the low-voltage operation is considered here to mean circuit operation at, or below, +3.3 V. The parameters considered in this paper are specifically the unity gain frequency (UGF), phase margin (PM) and the *rail-to-rail* input/output operation.

Rail-to-rail operation implies that the amplifier operates correctly to, or close to, the positive and negative power supply voltage levels and can be accomplished by using the *rail-to-rail* input/output circuit design techniques [1, 2]. In CMOS based circuits, the straightforward and common strategy for *rail-to-rail* operation of the input stage uses a p-channel MOSFET (metal oxide semiconductor field effect transistor) differential pair and an n-channel MOSFET differential pair connected in parallel. This arrangement is usually referred to as a *complementary input stage* [3]. However, as the input signal changes, the result will be a change in the total transconductance (g_{mTOT}) of the complementary input stage and this will affect the amplifier DC gain and frequency response. Ideally, the transconductance of the input stage is required to be constant over the entire input voltage range (from the lower power supply voltage (V_{SS}) to the upper power supply voltage (V_{DD})) in order to reduce signal distortion and to maintain circuit performance [4]. However, the effect of reducing the power supply voltage is to affect op-amp speed and margin of stability [5]. To overcome this reduction in performance, suitable amplifier compensation is required. Typically, Miller compensation, based on the use of a compensation capacitor around the output stage, is used to improve stability [6]. The addition of negative Miller compensation, which is also based on the Miller effect, can then improve speed (i.e., an increase in the UGF). The design has been created utilizing an AMS (Austria Mikro Systems) 0.35 µm CMOS (n-well) technology due to low-cost of fabrication along with pMOS and nMOS transistors available for 3.3 V and 5.0 V use with high current driving capabilities and excellent ESD performance [7].

In this paper, an op-amp architecture will be discussed which uses both conventional Miller and negative Miller compensation. Section 2 will discuss the complementary input stage circuit design and constant-g_m operation using a one-times current mirror and the structure of the output stage (class-AB amplifier). In section 3, amplifier compensation is presented, where negative Miller compensation is implemented around the first (complementary input) stage and conventional Miller compensation around second (output) amplification stage. Results of simulation studies using the Cadence Spectre

simulator will be presented in section 4, using a simulation strategy as identified in Figure 1. The op-amp study was therefore divided into three parts. Firstly, using the typical device model, a comparison of the op-amp performance with other reported work was undertaken. Secondly, the op-amp design was simulated with typical, worst-case power and worst-speed models and this provided an indication of the amplifier performance over the range of possible process parameter variations. Finally, the op-amp performance when connected directly to the vendor supplied standard input/output pads was simulated with the typical, worst-case power and worst-case speed models. The DC gain, UGF, gain-bandwidth product (GBP), PM and gain margin (GM) are considered as important performance parameters in this work. Section 5 will present a conclusion to the work.

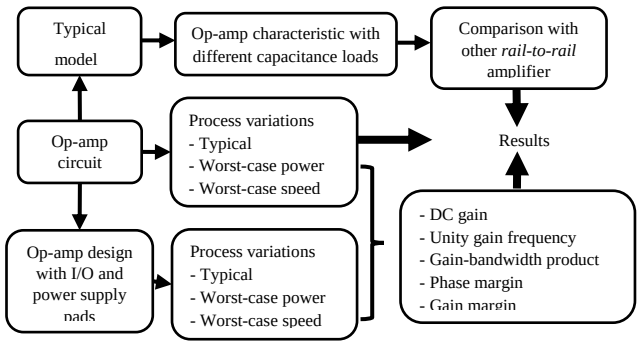

Figure 1. Design analysis simulation actions

II. DESIGN OF THE RAIL-TO-RAIL INPUT STAGE

Rail-to-rail op-amps are devices that can operate at, or close to, the circuit power supply voltage levels (or rails). "*Rail-to-rail*" operation can refer to the input, the output, or both input and output. "*Rail-to-rail*" is a term used to characterize an op amp whose dynamic range can reach the limits of the supply voltage. The dynamic range in a particular application is however dependent on how the op-amp is used. For example, with the op-amp output, the electrical load (typically a capacitance/resistance load) attached to the op-amp output will impact the dynamic range possible.

A. Design of the rail-to-rail input stage

The key principle of operation of the op-amp input stage is to amplify a differential input voltage and to reject any common mode input voltage [8]. A significant specification of the input amplification stage is the common mode input range [5]. The common mode input range is the range of the input DC voltage level at which all transistors in the input stage are in their active [9] (*saturation*) region. The most common circuit design technique to realise an input stage for single supply (*single-rail*) op-amp uses a parallel connection of pMOS (p-channel MOSFET) and nMOS (n-channel MOSFET) transistors in a differential input stage configuration. This technique combines the benefits of both transistor arrangements to accomplish *rail-to-rail* input performance [1]. Both input transistor pairs can be an arrangement as shown in Figure 2. A pMOS input pair is presented as M1-M2 and an nMOS input pair as M3-M4. The input common mode voltage for the nMOS transistor pair is from the positive power supply voltage (V_{DD}) down to ($V_{GSn} + V_{ds(sat)}$) above the negative power supply (V_{SS}). This is the minimum voltage required to maintain the nMOS transistors in the differential pair and the tail current source transistor (M7) in saturation. Figure 2 however assumes designer control over the transistor substrate (bulk) connection.

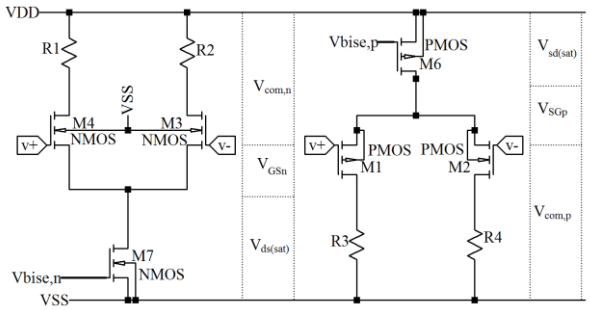

Figure 2. Common mode input range of pMOS and nMOS transistor differential pairs showing resistive loads with nMOS transistor bulk connections to V_{SS} in an n-well process

The common mode input voltage range for a nMOS transistor ($V_{com,n}$) is given by:

$$V_{SS} + V_{ds(sat)} + V_{GSn} < V_{com,n} < V_{DD} \quad (1)$$

$V_{ds(sat)}$ is the drain-source saturation voltage of transistor M7, V_{GSn} is the gate-source voltage of the nMOS input transistor. A comparable analysis can be performed for the pMOS differential pair shown in Figure 2. The range extends from ($V_{SGp} + V_{sd(sat)}$) below the positive power supply voltage down to the negative supply. This minimum voltage is required to maintain the tail current transistor (M6) in saturation. The common mode input voltage range of a pMOS input is then:

$$V_{SS} < V_{com,p} < V_{DD} - V_{sd(sat)} - V_{SGp} \quad (2)$$

where $V_{sd(sat)}$ of M6 is a minimum voltage between the transistor source and drain connections necessary for the transistor to operate in the saturation region, V_{SGp} is the source-gate voltage of the pMOS input transistor. Combining both differential pairs to reach complementary input stage shown in Figure 3, the common mode input (V_{com}) will vary as:

$$V_{SS} + V_{ds(sat)} + V_{GSn} < V_{com} < V_{DD} - V_{sd(sat)} - V_{SGp} \quad (3)$$

To ensure the common mode range can be *rail-to-rail*, the minimum supply voltage must be at least [5, 10].

$$V_{sup(min)} = V_{SGp} + V_{GSn} + V_{sd(sat)} + V_{ds(sat)} \quad (4)$$

The minimum power supply voltage ($V_{sup(min)}$) required to operate a MOSFET in saturation is usually formed by two parameters, the transistor threshold voltage V_T and the saturation voltage. If the power supply voltage in equation 4 is this minimum value, the common mode input voltage range will be identified by three regions of operation. These regions are also related to the MOSFET transconductance. The total

transconductance (g_{mTOT}) of the complementary stage in Figure 3 is shown in Figure 4 by the sum of the transconductances of the nMOS (g_{mN}) and pMOS (g_{mP}) differential pairs. Whilst there are three different regions of operation to determine g_{mTOT} as shown in Figure 4, the transconductance of the *rail-to-rail* CMOS input stage is a function of V_{com} [11]:

- Low $\mathbf{V_{com}}$; only the p-channel input pair operates.
- Intermediate $\mathbf{V_{com}}$; the p-channel as well as the n-channel input pair operate.
- High $\mathbf{V_{com}}$; only the n-channel input pair operates.

Therefore, at least one of the two differential pairs will be operated for any V_{com} between the power supply rails.

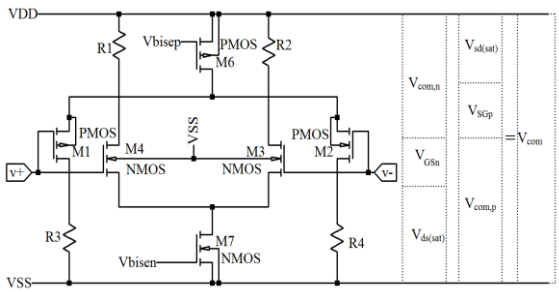

Figure 3. Common mode input range of a *rail-to-rail* input stage [5]

Assuming that the g_{mP} and g_{mN} are equal for the transistors operating in their saturation regions, an important issue in the design of the simple complementary input stage shown in Figure 3 is that the g_{mTOT} [5] is a result of the complementary input pairs working in the intermediate region. This is where both the pMOS and nMOS transistors contribute to the input stage transconductance. The gm_{TOT} of the input stage in this region is given by:

$$g_{mTOT} = g_{mN} + g_{mP} = 2g_m \quad (5)$$

The input stage can vary by a factor of 2 [10, 12] over V_{COM} and therefore frequency compensation cannot be optimized. Moreover, in the middle part of V_{com}, both input pairs are active and the sum of their drain currents is two times the current in the outer part of the V_{com}, when only one of the input pairs is active [13].

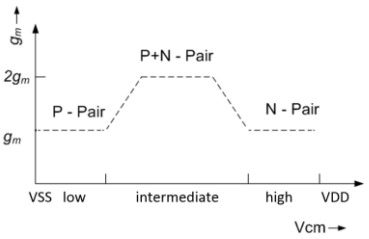

Figure 4. Transconductance g_{mTOT} versus the common mode input voltage for a *rail-to-rail* complementary input stage [14]

To achieve power-optimal frequency compensation, g_{mP} and g_{mN} must be controlled to be a constant value [5]. There are different techniques to operate input stages with a *rail-to-rail* common mode range and to equalize g_{mTOT}. Operating the transistor in a weak inversion, g_{mTOT} can be kept constant by keeping the sum of the tail currents constant, whereas in strong inversion, g_{mTOT} can be maintained constant by keeping the sum of the gate-source voltages constant [14]. The total transconductance is possible when the transistors operate in three different inversion regions of saturation. These are defined as *weak inversion*, *moderate inversion* and *strong inversion*. In these regions which can be controlled total transconductance as constant, as following:

1. if the transistor operates in *weak inversion*, the total g_m is given by:

$$g_{m\,TOT} = \frac{I_p}{2n_p V_{th}} + \frac{I_n}{2n_n V_{th}} \quad (6)$$

Where V_{th} is the thermal voltage kT/q, which is around 25.9 mV at room temperature (300 K) [15]. The values n_p and n_n are the weak inversion slope factor for the pMOS and nMOS transistors respectively. In the weak inversion, g_m can be controlled by changing the tail current of the input stage (complementary stage).

2. If the transistor operates in the *strong inversion*, the total g_m can use the square law models that lead to the total transconductance:

$$g_{mTOT} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_n} + \sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_p} \quad (7)$$

$$g_{mTOT} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n V_{gsn\,eff} + \mu_p C_{ox}\left(\frac{W}{L}\right)_p V_{sgn\,eff} \quad (8)$$

In equations 6 and 8, the total transconductance can be controlled by the tail current of the complementary input or by the transistor width (W) over length (L) ratios (i.e., the transistor dimensions) or by the gate-source voltage.

3. If the transistor operates in the *moderate inversion*, the total g_m is controlled by the transistor in a region between the *weak inversion* (low current) and the *strong inversion* (high current).

In this paper, the bulk of each nMOS transistor is actually connected to the V_{SS} (ground) node as the fabrication process is an n-well CMOS process. The bulk (body) is the p-substrate, and the source is n-type. The Body effect (or Substrate Bias Effect) denotes to the change in the transistor threshold voltage (V_T) with a voltage difference between the source and the bulk (V_{BS}) caused by a change in the width of the depletion layer. In an n-well process, the nMOS transistors share the same the substrate and the body of all the nMOS transistors are connected to the same voltage, typically the lowest voltage in the circuit (V_{SS}). However, pMOS transistors are built into the n-well and can be separated physically from each other. Each well can be biased to a different voltage. To avoid the body effect for a pMOS transistor, the transistor bulk and source would need to be connected together, as would be possible in a twin-well CMOS fabrication process. In this paper, the constant-g_m *rail-to-rail* input stage controlled by a tail current

using a current switch transistor will be considered. The current switch transistor uses a pMOS transistor and will be connected to the tail current of p-channel differential input stage and tail current of the n-channel differential input stage. The technique used to control the g_m variation problem is described in the next section.

B. Constant-g_m rail-to-rail input stage using a one-times current mirror

The total transconductance can be controlled by the tail current of the complementary input (see Figure 5). The complementary input transistors can operate in *strong*, *moderate* or *weak inversion*. However, *weak inversion* operation would allow the potential to minimize the power supply voltage. Assuming threshold voltages of 0.7 V and 0.5 V for the pMOS and nMOS transistors respectively, for a transistor saturation voltage of about 0.2 V, a minimum power supply voltage of 1.6 V would be required according to equation 4. To achive a minimum power supply voltage, the input stage must operate its transistors in *weak inversion*. When the g_m of a *rail-to-rail* input stage is working in *weak inversion*, the sum of tail currents of the complementary input (pMOS and nMOS) pairs used made constant [4, 5]. M1-M4 are complementary input pairs and a summing circuit consists of transistors M13-M18. g_m control of the input stage is implemented by current switch M5 and current mirror using transistors M7-M8.

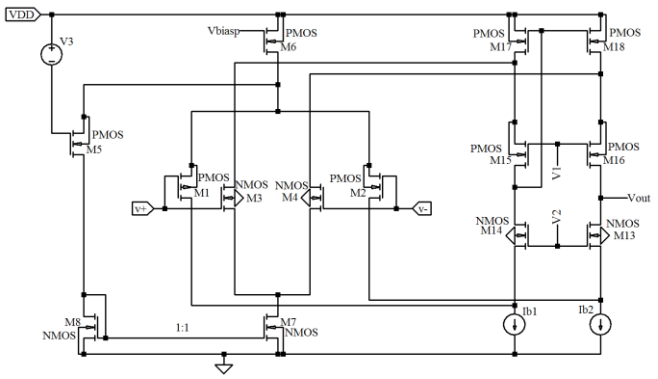

Figure 5. g_m control by a current switch and current mirror (1:1)[5]

The value of voltage V3 must be a half of the supply, and the W/ L ratio of M5 has to be made small when compared to the input transistor dimensions [5, 16]. If the common mode input range voltage is increased, the current of the p-channel input pair (I_{REF}) would be through the current switch to the current mirror and then feeds the n-channel input pair. The currents in the input stage will obey to total g_m as given by equation 5 when the g_m of input stage in *weak inversion* (Figure 6). Moreover, the transistors M1-M4 operate in weak inversion [17]. For achieving a high g_m, the transistor drain current must be increased. However, increasing this current may push the device into *strong inversion*, and this must be avoided to maintain low voltage operation. However, to keep the device in the low voltage mode by modifying the W/L ratio, the increased device geometries lead to increased device parasitic capacitances, thus affecting the high-frequency performance [16].

The key advantages of g_m control by a current switch are[18]:

1. It has a small circuit size and low power consumption. g_m control hardly increases the size of the input stage as the current switch and current mirrors are small [2].
2. g_m control does not increase the noise of the input stage as the noise generated by the g_m control circuit is inserted into the tails of the complementary input pairs, and thus can be considered as a common mode signal.

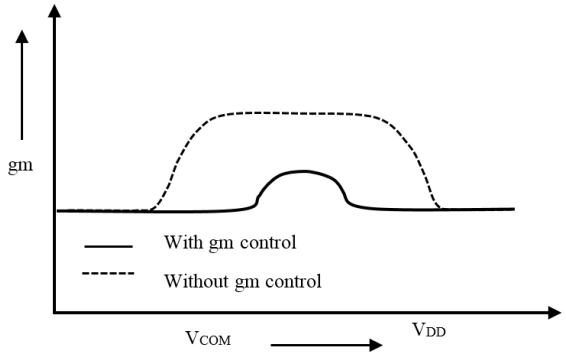

Figure 6. Transconductance (g_m) vs. common mode input voltage for the *rail-to-rail* complementary input stage with g_m control and without g_m control

C. Class-AB output stage

The output swing of an op amp describes how close the output of the op-amp can be operated to the negative or positive supply rails under defined operating and load conditions [1]. The advantage of the class-AB output is that it is capable of operating at high speed and close to the power supply voltage levels [19]. In order to achieve the *rail-to-rail* output, the output transistors M27-M28 must be in the common-source configuration with control transistors M19-M20 [17, 20, 21]. In Figure 7, feed-forward class-AB control is achieved by transistors M19 and M20. These transistors are biased by two signal currents from cascode transistors M13 and M16, and their V_{GS} values are kept constant by the connection of transistors M23-M24 and M25-M26. The floating current source (transistors M29-M30) has the same design as the feed-forward class-AB control, whose quiescent current is made less sensitive to supply voltage changes by using current mirrors biased independently. Therefore, transistors M17, M30, M25, M26 and M12, M29, M23, M24 generate two translinear loops that control the [14] value of the floating current source. Miller compensation has been incorporated between the gates of transistors M27 and M28. The amplifier phase margin is limited by the two compensation capacitors, CM1 and CM2, which separate the amplifier poles to provide a first-order gain characteristic. The transistor coupled class-AB control is beneficial in that [5]:

1. No noise or DC offset voltage added to the first stage of the amplifier.
2. A good high-frequency behavior is accomplished due to the connection between the gates being achieved by a single transistor.
3. It should not reduce the open-loop gain of the amplifier. The class-AB control transistors do not decrease the gain of the amplifier.

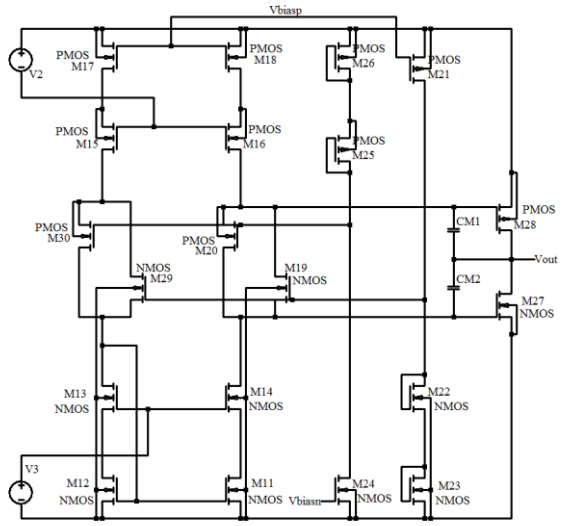

Figure 7. Circuit diagram of the low-voltage class-AB output stage

III. MILLER AND NEGATIVE MILLER COMPENSATION

The basic idea of the Miller effect is that if the inverting amplifier has a feedback capacitance between the output and input as shown in the Figure 8 (a), the Miller effect creates equivalent circuits as presented in Figure 8 (b). The inverting amplifier gain (A) is as defined as being negative. The Miller effect will then show on the input node ($C_{1(Miller)}$) and output node ($C_{2(Miller)}$) with respect to ground.

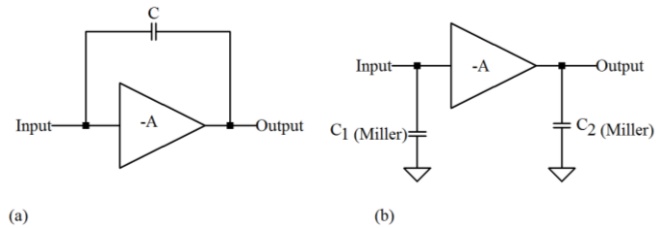

Figure 8. Concept of Miller (a) Inverting amplifier with Miller capacitor, (b) Equivalent circuit using Miller theory

The negative capacitance technique is based on Miller effect theory, which also describes the impact of the feedback capacitance on the input capacitance as shown Figure 9. In this method, the capacitor is connected around non-inverting with a gain, A >> 1. The input capacitance, C_I, of the amplifier with no feedback capacitance would affect the frequency of response of the amplifier. The feedback capacitance (C_{NM}) is formed around the non-inverting amplifier and the effective input capacitance (C_I') with the negative Miller can be written as:

$$C_I' = C_I + (1 - |A|)C_{NM} \quad (9)$$

If C_{NM} is significant when compared to C_I, there will be an effect of negative capacitance or an equivalent inductive effect over a narrow frequency band [22, 23]. However, as the single gain stage is usually inverting [24], the op-amp will need to designed to implement a non-inverting stage (Figure 10). The sign in the parenthesis goes negative, decreasing the input capacitance. Such a property might be utilized to improve the bandwidth. A limitation of this technique is that the feedback capacitors are shown an additional load for the output stage, which could decrease the bandwidth.

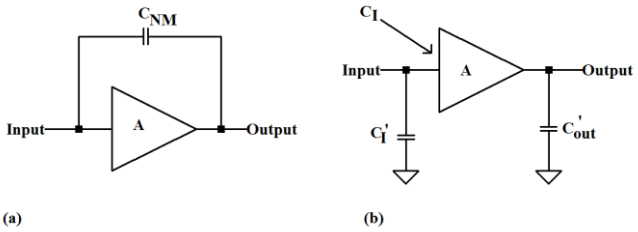

Figure 9. Concept of negative Miller (a) Non-inverting circuit with negative Miller capacitor, (b) Equivalent circuit

Additionally, the stability of the design must be confirmed as if the feedback capacitors are too large, the overall capacitance of the input stage may become negative [24]. In [25], the manner in which to obtain a negative Miller around a buffer, and to reduce the effective load capacitance to achieve both a higher bandwidth and improved PM, is shown. Figure 11 is the proposed design for connecting the negative Miller compensation used in this paper.

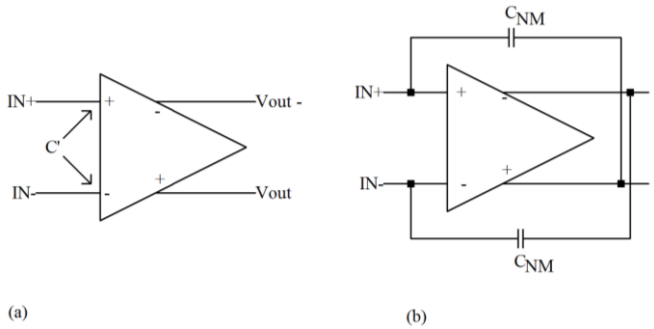

Figure 10. Fully differential stage (a) Without and (b) With negative Miller capacitances

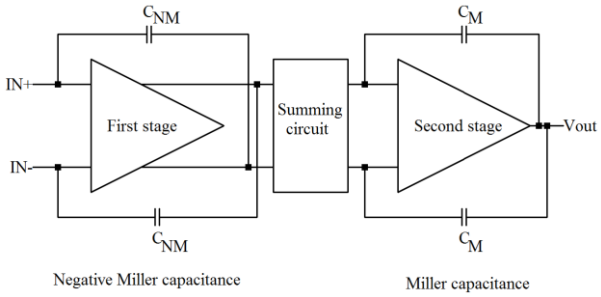

Figure 11. Op-amp single ended using negative miller compensation around the first stage (proposal)

The negative Miller compensation is connected around the first stage of op-amp since the first stage provides a differential input and a differential output. This way reduces, or cancels, part of the effect of input capacitance and hence improve the frequency response. In the meantime, the conventional compensation (Miller capacitor, C_M) is used to improve the stability of op-amp and it is used connected around the second stage.

IV. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The proposed op-amp design utilities both conventional Miller and negative Miller compensation techniques and is implemented in a 0.35 µm CMOS process. Figure 12 shows the two-stage op-amp with the single ended output. The input amplifier represents the differential pair amplifier with summing circuit and amplifier represents the class-AB amplifier. The compensation circuit has been around the first stage and called negative Miller and the other compensation around second amplification. As well as, the g_m control by a current switch is employed to achieve inputs and outputs of the *rail-to-rail* op amp. With this particular design, the DC power consumption is 2.311 mW.

Table I identifies the op-amp performance. For the transient analysis, the *pulse* input was used at 0 V/+3.3 V levels with a 50% duty cycle at a frequency of 1 MHz and the signal applied to the op-amp in a unity gain configuration. With this arrangement, the low and high output voltages are 1.73 mV and 3.295 V respectively.

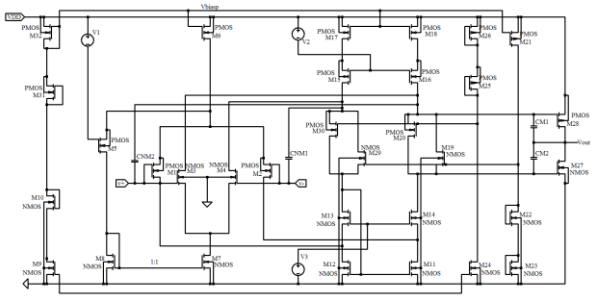

Figure 12. Structure of the two-stage *rail-to-rail* op-amp

TABLE I. PERFORMANCE SUMMARY (SIMULATION RESULTS USING THE TYPICAL MODEL)

Performance	Value
Technology (µm)	0.35
Power supply (V)	3.3
DC gain (dB)	85.33
Unity gain frequency (MHz)	271.1
Phase margin (degrees)	63.78
Gain-bandwidth product (MHz)	206.7
Slew rate (V/µs)	661.23
Settling time (µs)	0.205
Common mode input range (V)	0~3.3
High output voltage (V)	3.295
Low output voltage (mV)	1.73
Input bias current (µA)	62.8
Power consumption (mW)	2.311
Area (µm)	120.4*121.5

Table II presents the results of the simulation approach and results obtained focused on the frequency response by using the op-amp with different an output load capacitance with values of 0.1 pF, 0.5 pF and 1.0 pF. The capacitive load has impact on the UGF and PM, which decreases with increasing load capacitance (C_L). The result of the capacitive load stability issue in op-amp is a transfer function pole modeled by the load capacitance and the open-loop output impedance of the op-amp. This output pole increases the phase lag around the loop that decreases the PM. The load resistance has a minor impact on the op-amp performance. If the load resistance is reduced all the way to 0 Ω, the output voltage will be limited to the short circuit value. The result is that the open-loop gain and the frequency response are decreased.

TABLE II. OPEN-LOOP OP-AMP CHARACTERISTIC WITH DIFFERENT LOAD CAPACITANCE VALUES (SIMULATION RESULTS USING THE TYPICAL MODEL)

Performance	No load	0.1 pF	0.5 pF	1 pF
DC gain (dB)	85.33	85.33	85.33	85.33
Unity gain frequency (MHz)	271.8	264.4	233.8	214.3
Phase margin (degrees)	63.62	61.42	46.6	49.09
Gain-bandwidth product (MHz)	206.7	206.7	206.7	206.7
High output voltage level (V)	3.298	3.298	3.298	3.298
Low output voltage level (mV)	1.73	1.73	1.73	1.73

Table III shows the results of the simulation approach and results focused on the frequency response by using the op-amp with different output load resistances with values of 0.1 kΩ, 1 kΩ, 10 kΩ and 1 MΩ with 0.5 pF parallel load capacitance.

TABLE III. OPEN-LOOP OP-AMP CHARACTERISTIC WITH DIFFERENT LOAD RESISTANCE VALUES (SIMULATION RESULTS USING THE TYPICAL MODEL)

Performance	R_L (C_L = 0.5 pF)			
	0.1 kΩ	1 kΩ	10 kΩ	1 MΩ
DC Gain (dB)	43.43	66.133	80.89	85.27
Unity gain frequency (MHz)	29.91	160.10	224.5	233.6
Gain-bandwidth product (MHz)	29.52	148.52	198.7	206.5
Gain margin (dB)	22.45	-9.34	-7.22	-6.979
Phase margin (degree)	86.07	69.70	56.82	54.68
High output voltage level (V)	1.93	3.133	3.283	3.295
Low output voltage level (mV)	1.73	1.73	1.73	1.73

In Table IV, the simulated op-amp performance (TM) is compared to four reported op-amp designs operating at the same power supply voltage (i.e., +3.3 V). The simulation results were obtained using BSIM3v3 transistor models, typical process values and no output load. The design combines negative Miller and conventional Miller compensation and demonstrates an improvement in the frequency respose at a power supply voltage (+3.3 V) using a standard 0.35 µm CMOS process. A comparison was also made with the other previous op-amp designs [27], [28], [29], and [30], where these designs have been designed for particular applications. As shown in Table 4, the proposed op-amp has a larger static power consumption than the previous designs, but low-power was not a design constraint in this design. The power consumption increases rapidly with increased UGF [26]. The UGF achieved from the circuit is significantly higher, but at the cost of reduced PM.

TABLE IV. COMPARISON WITH REPORTED *RAIL-TO-RAIL* OP-AMP DESIGNS

Performance	Reported work				
	2002[27]	2004[28]	2017[29]	2015[30]	This work
Technology (µm)	0.35	0.35	0.35	0.35	0.35
Power supply (V)	3.3	3.3	3.3	3.3	3.3
DC gain (dB)	65	74.2	89.8	70	85.33
Load capacitance (pf)	600	No	No	No	1
Unity gain frequency (MHz)	0.75	0.008	No	9.5	214.3
Phase margin (degrees)	50	81.9	59.5	73	49.09
High output voltage level (V)	3.25	3.28	2.72	3.29	3.298
Low output voltage level (mV)	50	20	198.7	0	1.73
Power consumption (mW)	No	0.00055	No	0.96	2.311

A. AC and transient analysis

The open-loop frequency response of the op-amp is presented in Figure13 (gain and phase). The design was simulated using the typical model with no output load. The open loop gain magnitude is 85.27 dB and the unity gain frequency is 271.8 MHz with a phase margin 63.62°. Figure 14 shows the open-loop gain magnitude changes with load resistance. This can be seen to reduce with a reducing load resistor value. For example, the gain magnitude is 43.43 dB with a load resistance of 100 Ω. In addition, the phase of the circuit with the different load resistance values.

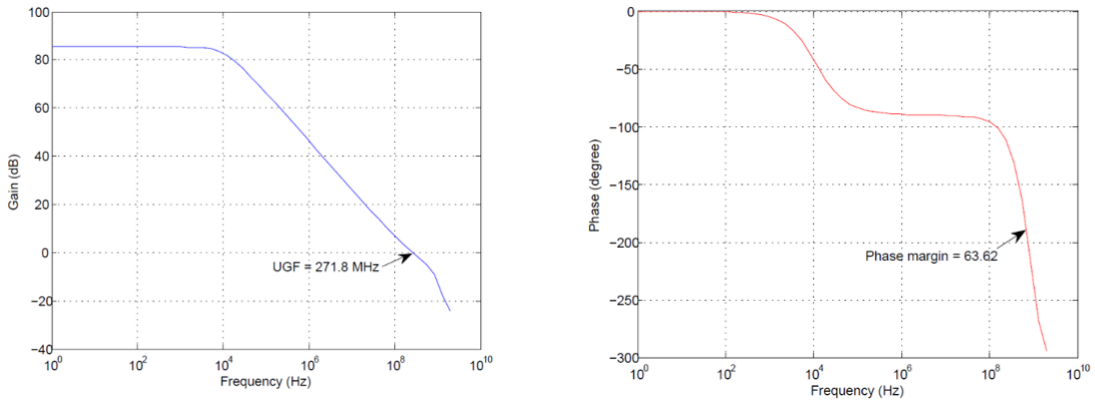

Figure 13. Frequency response of open-loop op-amp gain magnitude and phase (simulation results using the TM)

The transient response is shown in Figure 15. The input signal is a PULSE waveform that varies between 0 V and 3.3 V with period of 1 µs. The maximum output voltage level is 3.295 V and the minimum output voltage is 1.73 mV.

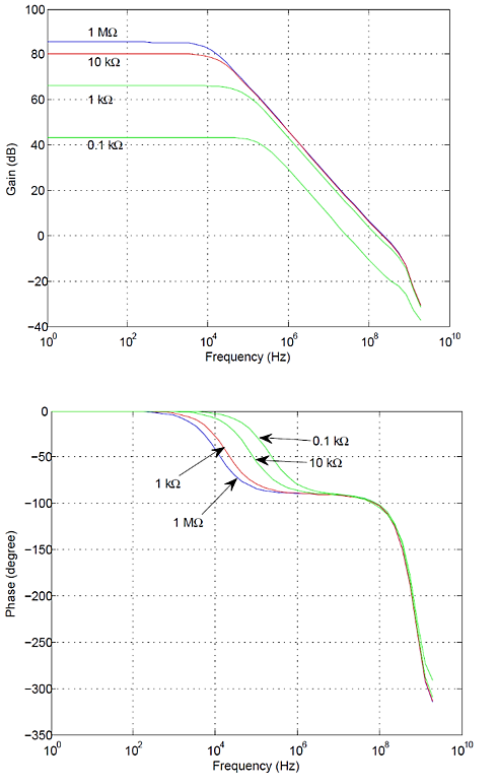

Figure 14. Frequency response of open-loop op-amp gain magnitude (and phase) with load resistance (simulation results using the typical model)

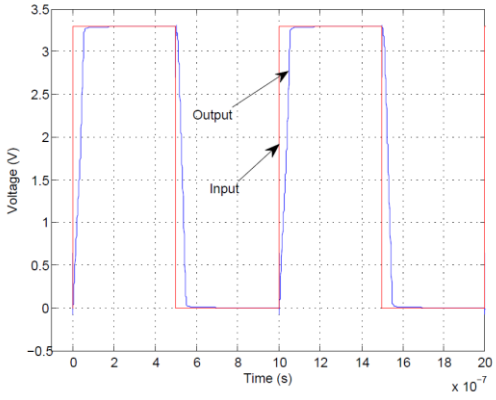

Figure 15. Step response (red trace: input; red blue: output) (simulation results using the TM)

The input signal is applied to the non-inverting node of the input stage with the simulation study based on the op-amp in a unity gain configuration. From Figure 15, the slew rate can be extracted. Slew rate (SR) is described as the maximum rate of change of output voltage per unit of time and is expressed as volt per second and in this case is approximately 661.23 µs/V. In addition, DC analysis results are shown in Figure 16. The DC analysis was undertaken again using a unity gain configuration where the DC simulation was undertaken where the input voltage was swept from 0 V to 3.3 V. The *VOUT vs. VIN* characteristic was plotted in order to determine the input common mode voltage, the range of input voltage where the circuit has a gain of approximately one. The input common mode is rail-to-rail as well as producing low and high output voltages of 1.73 mV to 3.295 V, respectively.

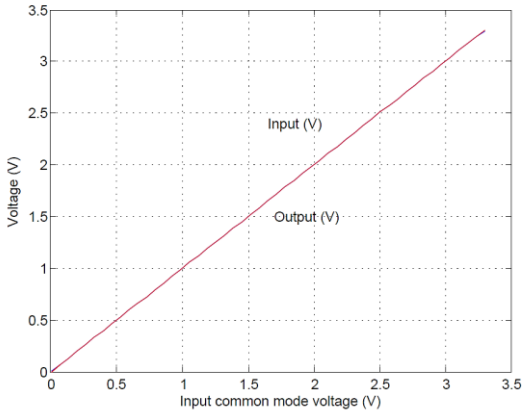

Figure 16. DC performance of the op-amp in non-inverting unity-gain configuration (simulation results using the TM)

The circuit technique providing a constant-g_m *rail-to-rail* input stage uses a one-times current mirror. Figure 17 shows how the transconductance varies with the common mode input voltage where the total transconductance (g_{mTOT}) is the combined effect of both g_{mN} for the nMOS and g_{mP} for pMOS input transistors. The constant-g_m simulation results over whole the common mode input range was also identified with the transistors operating in weak inversion.

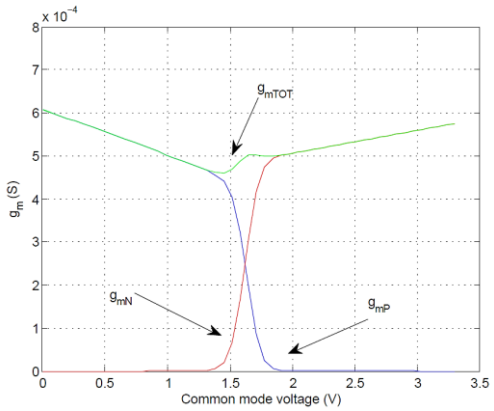

Figure 17. g_m control by a current switch and current mirror (1:1) versus common mode (simulation results using the TM)

B. Corner Analysis with I/O pads

The expression 'Process Corner' denotes to the variations in the performance metrics due to manufacturing variations [29]. The process corners are considered where the op-amp is simulated with worst case power (WP) and worst-case speed (WS) device models and the Spectre simulation models for the process devices provided this corner data. That means, the typical model is where the nMOS and pMOS transistors operate at normal speed, worst-case speed means slow nMOS and slow pMOS transistors, and worst-case power means fast nMOS and fast pMOS transistors. The *pad* is used to connect the op-amp circuitry within the IC to the IC package and would also to contain circuitry, primarily for electrostatic discharge (ESD) protection. The pads are a semiconductor fabrication which these protection devices show capacitances and resistances to the signal path, and at higher frequencies, the pad capacitances will provide low impedance paths to ground [31].

The operation of the op-amp was evaluated in simulation using Cadence Spectre simulations and considering physical process variations. The simulation results, as shown in Table V, identify that for the op-amp with typical model operating on a 0 V/+3.3 V power supply voltage, the DC gain is 85.33 dB, the phase margin is 63.78°, and the unity gain frequency is 271.1 MHz. In Table 5, the op-amp simulation results are shown for typical and also worst-case process models. In Table VI, the op-amp frequency response with different process variations and considering the effects of the I/O pads are presented. For the typical model, the unity gain frequency reduces to 187.4 MHz, the gain-bandwidth product is marginally reduced to 206.5 MHz, the gain margin becomes -8.606 dB and the phase margin is now 45.05°. The DC gain for the typical model is 85.33 dB, 33 dB for worst-case power and 93.94 dB for worst-case speed, which are only marginally different to the results presented in Table V. The I/O pads have only a marginal effect on DC gain, high output voltage and low output voltage. In this part of the simulation study, the output pad provided the only electrical load for the op-amp and no electrical load was connected to the output of the output pad.

C. Op-amp layout considerations

The design layout is based on an n-well CMOS technology where the substrate of an nMOS transistor is always connected to V_{SS}. As the nMOS and pMOS transistors are fabricated into the same wafer, Figure 18, in an n-well CMOS technology then the p-substrate is the substrate for the nMOS transistor and the n-well is the substrate for the pMOS transistor. The pMOS transistor bulk is isolated from the substrate and therefore can be connected to the source. In contrast, the bulk of the nMOS is the substrate itself and thus the bulk of the nMOS cannot always be connected to the source. If the transistor bulk connects to its source, all the sources of the different nMOS transistors will be connected to each other [32].

TABLE V. PROCESS VARIATIONS OF OP-AMP WITHOUT I/O AND POWER SUPPLY PADS

Performance	TM	WP	WS
DC gain (dB)	85.33	32.99	90.82
Unity gain frequency (MHz)	271.1	488.4	56.28
Gain-bandwidth product (MHz)	206.7	403.3	41.14
Gain margin (dB)	-6.737	-9.095	-8.85
Phase margin (degrees)	63.78	74.77	76.47
High output voltage level (V)	3.291	3.23	3.290
Low output voltage level (mV)	1.73	135.97	3.931

TABLE VI. SIMULATION OP-AMP WITH THE I/O AND POWER SUPPLY PADS

Performance	TM	WP	WS
DC gain (dB)	85.33	33	93.94
Unity gain frequency (MHz)	187.4	383.8	45.77
Gain-bandwidth product (MHz)	206.5	371.4	40.77
Gain margin (dB)	-8.606	-11.12	-9.374
Phase margin (degrees)	45.05	63.54	60.73
High output voltage level (V)	3.291	3.23	3.290
Low output voltage level (mV)	1.78	135.97	3.931

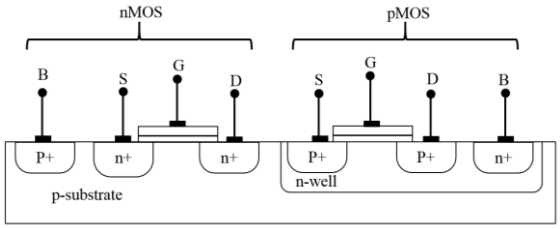

Figure 18. An n-well CMOS process identifying the nMOS and pMOS transistor connections

The layout of the circuit shown in Figure 19 (a) was created using Cadence Virtuoso. The layout size is 120.4 * 121.5 µm. The connections between the transistors (nMOS and pMOS) and capacitors (polysilicon-polysilicon capacitors) are made in *metal 1*, *metal 2* and *polysilicon 1* layers. The op-amp circuit is surrounded by two guard rings (the inner guard ring is connected to V_{SS} and the outer guard ring is connected to V_{DD}). Figure 19(b) shows a block diagram representation of the layout in Figure 21 showing the positions of the different circuit building blocks. This shows the input, summing circuit and output stages in addition capacitors layout for the negative Miller and Miller capacitors. The devices are placed in layout as a symmetry group. The larger the distance between the symmetry pair, the greater differences between their electrical properties. It was therefore important for the symmetric devices of a symmetry group to be placed in close proximity.

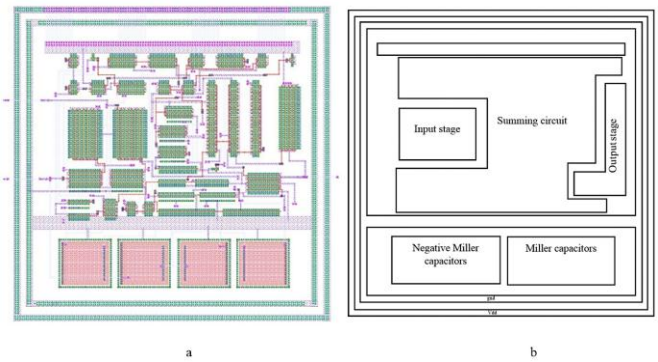

Figure 19. a) Block diagram representation of the op-amp layout, and b) Layout of the rail-to-rail input/output op-amp

Table VII presents the results of the op-amp that it has been simulated without I/O and power supply pads. The circuit simulations take into account the layout parasitic effects. The parasitic effects taken into account are capacitances (C) only and resistance-capacitance (RC). The design was simulated using the typical process model. In RC parasitic, the DC gain is reduced to 58.89 dB while the capacitance only does not affect the DC gain which is 85.33 dB. The UGF is decreased to 159 MHz whilst the unity frequency is 228.1 MHz when the take into account capacitance effect only. In addition, the GBP is 136.6 MHz while the simulation with capacitance only is 22.1 MHz. The GM has been increased to -9.543 dB. In RC extraction, the range of the high output voltage level and low output voltage level is 3.294 V and 2.096 mV respectively.

TABLE VII. SIMULATION OP-AMP WITH LAYOUT PARASITIC EXTRACTION OF SCHEMATIC WITHOUT I/O AND POWER SUPPLY PADS (TYPICAL MODEL)

Performance	No parasitic RC	RC	C
DC gain (dB)	85.33	58.91	85.33
Unity gain frequency (MHz)	272.9	159	228.1
Gain-bandwidth product (MHz)	206.7	136.6	201.8
Gain margin (dB)	-6.737	-9.543	-7.65
Phase margin (degrees)	63.78	64.58	52.91
High output voltage level (V)	3.291	3.294	3.295
Low output voltage level (mV)	1.73	2.096	1.73

The design was simulated with layout parasitic component extraction for both op-amp circuit and I/O and power supply pads as shown in Table VIII. The effects are most noticeable with the DC gain that is reduced to 58.91 dB with the typical model and the UGF has been reduced to 110.4 MHz. In addition, the GBP is decreased to 136.3 MHz and phase margin is reduced slightly to 45.54°. However, the GM is increased to -11.36 dB. The high output voltage level remains constant, but the low output voltage level is increased slightly to 2.09 mV.

Generally, the UGF, GBP, GM and PM follow the expectation that the parasitic capacitances have more of an effect at higher frequencies since the capacitance reactance decreases with an increase in frequency. The DC gain has not been effected by parasitic capacitance influence as the capacitance at low frequency acts as open circuit. In addition, the DC gain has been effected by parasitic resistances. Gate series resistance is the most significant resistive parasitic that needs to be considered. A large gate series resistance significantly reduces the UGF and gain [33], along with additional parasitic resistances such as source-drain resistance and via resistances [34].

TABLE VIII. SIMULATION OP-AMP WITH LAYOUT PARASITIC EXTRACTION OF SCHEMATIC AND PADS (TYPICAL MODEL)

Performance	No parasitic RC	RC	C
DC gain (dB)	85.33	58.91	85.33
Unity gain frequency (MHz)	187.4	110.4	144.5
Gain-bandwidth product (MHz)	206.5	136.3	201.5
Gain margin (dB)	-8.606	-11.36	-7.833
Phase margin (degrees)	45.05	45.54	31.29
High output voltage level (V)	3.291	3.29	3.28
Low output voltage level (mV)	1.78	2.09	1.366

V. CONCLUSION

In this paper, a two-stage CMOS *rail-to-rail* input/output op-amp operating on a +3.3 V single rail power supply voltage that incorporates negative Miller and Miller internal compensation was presented. The op-amp was designed using 0.35 µm, n-well CMOS process and its operation was verified in simulation using Cadence Spectre. The design architecture and compensation scheme were chosen to improve the frequency response and stability with respect to phase margin, unity gain frequency, gain-bandwidth product and gain margin. A *rail-to-rail* input/output design was a requirement for this op-amp. The input stage was based on the constant-g_m circuit using a one-times current mirror. In addition, the output was established using a class-AB output stage. The design operation was simulated using three different process models (typical, worst-case speed and worst-case power) in order to understand the behavior of the op-amp with process variations and different output load conditions.

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